# A Seven Level inverter with Reduced Switch for Various PWM Strategies

K.Meenakshi, C.R.Balamurugan, S.P.Natarajan, T.S.Anandhi

**Abstract**— This paper presents a three-phase seven-level inverter with RL (Resistive and Inductive) load for various Bipolar Pulse Width Modulation (BPWM) strategies are like Phase Disposition (PD), Phase Opposition and Disposition (POD) PWM, Alternative Phase Opposition and Disposition (APOD) PWM, Carrier Overlapping (CO) PWM and Variable Frequency (VF) PWM sinusoidal reference and trapezoidal reference. The independent work of this paper is equivalence of Total Harmonic Distortion (THD), VRMS and VPEAK for sinusoidal and trapezoidal references. The simulation performance is done through MATLAB /SIMULINK software. COPWM strategy is to perform better as of it provides relatively higher fundamental RMS output voltage.

**Index Terms**— PD, APOD, CO, VF, PWM, Total Harmonic Distortion.

## 1 Introduction

A MultiLevel Inverter (MLI) is relatively used in high voltage and high current applications. The desired stepped AC voltage waveform is obtained from several levels of DC voltage. It provides more advantages as compared with conventional two-level inverter which gives lesser switching losses and frequency. The smallest number of voltage/current levels for a multilevel inverter using cascaded inverter. When the number of levels increases eternity, the yield THD overtures zero. This attained number of voltage levels however confined by voltage unbalance problems, circuit setup, packaging restraints, initial and maintenance cost. Behera et al. (2010) introduces multilevel converter fed induction motor drive for industrial and traction drive has less voltage stresses, harmonics, and electromagnetic interferences. Modifications are made in its inbuilt structure.Malinowski et al. (2010) presented, cascaded multilevel inverters which allows one to achieve high quality output voltages and input currents and also outstanding availability due to their intrinsic component redundancy. Lezana et al. (2011) introduced hybrid multi-cell converter in which allows that no losses and high modularity. Floricau et al. (2011) presented a new multilevel converters based on stacked commutation cells with shared power devices. Kangarlu et al. (2012) presented a symmetric multilevel inverter with reduced components based on non-insulated dc voltage sources. Yousedfpoor et al. (2012) proposed an efficient approaching to reduce the harmonic contents of the inverter's output voltage by THD minimization. Rathore et al. (2013) evaluated an optimal pulse-width modulation of multilevel inverters for low-switching-frequency control and for harmonic control. Kui Wang et al. (2013) proposed a nine-level inverter which can get over the limitations of traditional neutral-point-clamped and flying capacitor converters. It can be naturally balanced beneath ideal and steady conditions. Ajami et al. (2014) introduced a cascade multi-cell multilevel converter and it has one advantage that to reduce THD. Buccella et al. (2014) proposed a procedure to eliminate harmonic components from inverter output voltage and, for each harmonic, return the exact boundaries of all valid modulation index intervals. Dayoodnezhad et al. (2014) presents the strategy uses the measured average of the switched phase leg output voltage to adjust the controller hysteresis band as the load back Electro Motive Force (EMF) varies to maintain a near constant phase leg switching frequency.

Hence this paper presents a new seven-level inverter which uses eight power switches. Output voltages are phase voltage VP and line voltage VL can be evaluated by this seven-level inverter.

## 2 Proposed MultiLevel Inverter

Multilevel inverter is a power electronic device which synthesis an AC voltage/current from desired sinusoidal waveform and actually it divides main DC supply to separate DC voltage sources. The proposed symmetrical multilevel inverter consists of three DC voltage sources (E1, E2 and E3) and eight power semiconductor switches with three-phase Resistive Inductive (RL) load. Three DC voltage sources are, E1=E2=E3=$V_{dc}$ and RL- load has 100Ω and 0.5mH. Proposed MLI needs only eight switches, but for Conventional Cascaded MultiLevel Inverter (CMLI) contains twelve switches to generate symmetrical seven-level inverter. Modes of operation can also be generated by its respective switching patterns.

Bipolar PWM strategies are used to compare the performance measures for both reference waveforms. Trapezoidal is advanced reference waveform while compared with sine reference waveform. Eight switches are $T_1$, $T_2$, $T_3$, $T_4$, $T_1'$, $T_2'$, $T_3'$ and $T_4'$. When uses of bi-directional switches are Metal Oxide Silicon Field Effect Transistor (MOSFET), Insulated Gate Bipolar Transistor (IGBT) and etc., the losses in switches should be decreased. The seven-level output voltages are +3Idc, +2$I_{dc}$, +$I_{dc}$, 0$I_{dc}$, -3$I_{dc}$, -$I_{dc}$ and -$I_{dc}$. This three DC voltage sources produces stepped or staircase waveform from an approximate AC sinusoidal waveform. All performance measures are obtained for both line voltage and phase voltage separately and output voltage waveform also be obtained.

The operation can be explained as: For +3$I_{dc}$ output switches $T_1$, $T_3$, $T_2'$ and $T_4'$ should be in ON position. For +2$I_{dc}$ output switches $T_1$, $T_3$, $T_4$ and $T_2'$ should be in ON posi-

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tion. For +Idc output switches $T_1$, $T_2'$, $T_3'$ and $T_4'$ should be in ON position. Same as for 0Idc output switches $T_1'$, $T_2'$, $T_3'$ and $T_4'$ should be in ON position. The negative polarity output voltages $-3I_{dc}$, $-2I_{dc}$ and $-I_{dc}$ are redundancy for positive polarity output currents. MLI has applications of adjustable speed drives and renewable energy sources (solar cell, Fuel cell, wind energy and etc.).

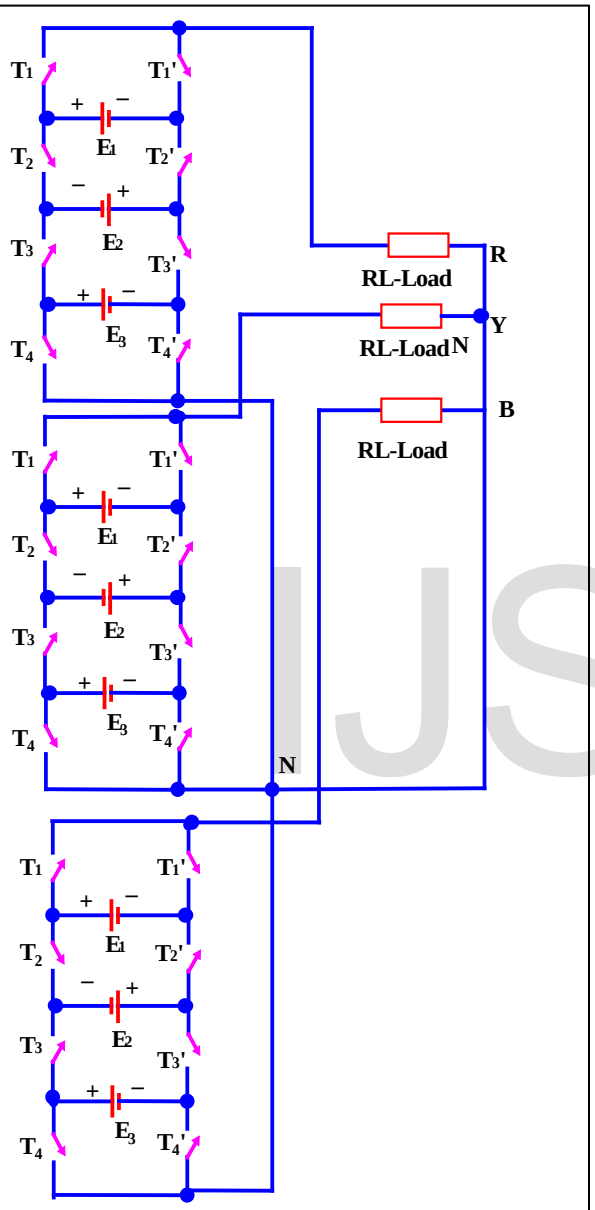


Fig. 1. Proposed three-phase seven-level inverter.

Figure 1 shows proposed three-phase seven-level inverter with three-phase Y (star) connected resistive inductive load. Therefore, to obtain the total ac voltage produced by the multilevel inverter, there seven distinct ac voltages are added together. The one notices that three distinct dc sources can produce a maximum of seven distinct levels in the output phase voltage of the proposed multilevel inverter.The voltage stress on each switch is decreased. Therefore, the rated voltage and consequently the total inverter power could be safely increased by increasing the resistive load value.

TABLE 1
SWITCHING TABLE FOR PROPOSED SEVEN-LEVEL INVERTER

| S. No. | Switching States | | | | | | | | Output Voltage |
|---|---|---|---|---|---|---|---|---|---|
| | $T_1$ | $T_2$ | $T_3$ | $T_4$ | $T_1'$ | $T_2'$ | $T_3'$ | $T_4'$ | |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | $+3I_{dc}$ |
| 2 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | $+I_{dc}$ |
| 3 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | $I_{dc}$ |
| 4 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 5 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | $-I_{dc}$ |
| 6 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | $-2I_{dc}$ |
| 7 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | $-3I_{dc}$ |

Three input dc sources with $E_1 = E_2 = E_3 = 50$ V are used. The switching table so obtained is shown in Table 1, which shows that switches $T_2$, $T_2'$, $T_3$ and $T_3'$ operate at a fundamental frequency of 50 Hz while switches $T_1$, $T_1'$, $T_3$, and $T_3'$ operate at a frequencyof 2 kHz. Thus, low-voltage-rated switches operate at high frequency and incur more switching losses, while high-voltage rated switches operate at fundamental frequency and incur more conduction losses. In this manner, the total losses among the switches get distributed. Switching losses are very directly proportional to the switching frequency. This paper evaluates THD, $I_{RMS}$ and $I_{PEAK}$ for both line voltage and phase voltage. Comparison of THD and RMS fundamental output voltage for sine and trapezoidal references can also be determined through FFT analysis.

## 3 SWITCHING SCHEME

High-switching-frequency modulation methods like multicarrier bipolar PWM and space vector modulation techniques have been used for MLI modulation control. The proposed topology can be modulated with any one of these methods with suitable adjustment. In the present work, the multicarrier bipolar PWM scheme is used. In a multicarrier bipolar PWM scheme, carrier signals are compared with the reference signal, and the pulses obtained are used for switching of devices corresponding to respective voltage levels. In the proposed topology, one switch may contribute for synthesis of more than one level at output terminals.

The modulating/reference wave of multilevel carrier based PWM strategies can be sinusoidal PWM signal. The reference wave is concerned for CFD including frequency, amplitude and phase angle of the reference wave. The following strategies are employed in this study. This switching table will lead to fundamental switching of $T_2$, $T_2'$, $T_3$ and $T_3'$ which bear voltage stress of $2V_{dc}$ each as compared to the remaining switches which bear voltage stress of Vdc each. This treatment

can, however, be extended for higher level inverters. In this various Bipolar PWM techniques but for only one sample technique Bipolar Phase Disposition (BPD) PWM is used. Because this technique generate reduced total harmonic distortion.

Bipolar multicarrier techniques with sine reference are as given: In Phase disposition technique, all the carriers are in phase with each other. For an m-level inverter using bipolar multicarrier technique, (m-1) carriers with the same frequency fc and same peak-to-peak amplitude Ac are used. The reference waveform has amplitude Am and frequency fm and it is ended at zero level. The three-phase sine reference wave is continuously compared with each of the carrier signal. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched on. Otherwise, the devices would be switched off. The frequency ratio mf is defined in the PWM strategy as follows:

$$m_f = \frac{f_c}{f_m}$$

The amplitude modulation index ma of this method is

$$m_a = \frac{A_m}{n * A_c}$$

Figure 2 shows the multicarrier arrangement for PDPWM method for $m_a = 0.9$ and $m_f = 40$.

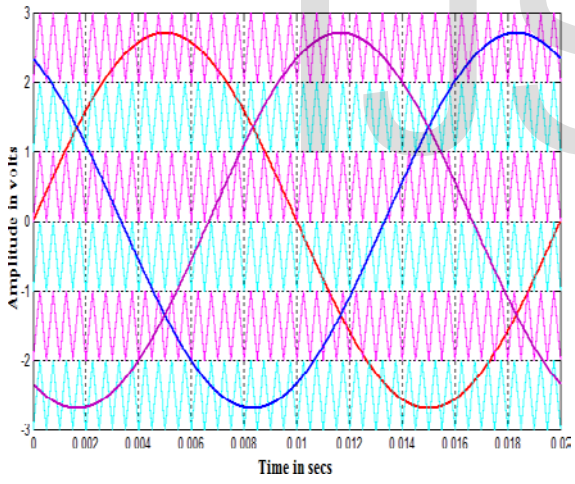


Fig. 2. Sine reference with bipolar carriers waveform for the proposed scheme for a seven-level output.

Same as of amplitude modulation index $m_a$ and frequency modulation index $m_f$ for trapezoidal reference with bipolar PDPWM technique. This technique is advanced technique while compared with sinusoidal reference. It gives lesser harmonic distortion, higher fundamental RMS output current, less DC component and higher peak current (fundamental). Figure 3 shows the multicarrier arrangement for PDPWM method for $m_a = 0.9$ and $m_f = 40$.

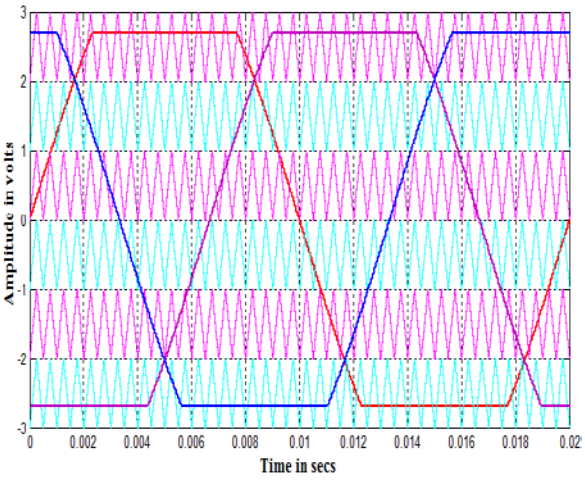


Fig. 3. Trapezoidal reference with bipolar carriers waveform for the proposed scheme for a seven-level output.

## 4 Simulation Results

The three-phase cascade seven-level inverter can be modeled in SIMULINK model by using power system block set. Switching signals for Cascaded Multi Level Inverter (CMLI) are developed using BPWM techniques but for only one sample technique BPDPWM is used. The power balancing among input dc sources is important so that all dc sources have equal lifetimes. Power balancing is also crucial when the DC sources are renewable sources such as PV cells.The simulation is performed for different values of ma ranging from 0.7-1. The corresponding %THD values and IRMS of fundamental and peak amplitude current IPEAK of inverter output for same modulation indices corresponding of FFT plots and they are shown in below tables. Below figures shows the simulated output current waveforms for a CMLI and corresponding FFT plots but for only one sample value of ma = 0.9. Tables 2 – 7 obtain the performance measures such as %THD, $I_{RMS}$, $I_{PEAK}$ and DC component. Figures 4 – 23 shows the three-phase output current (line) waveforms for sine and trapezoidal references and its respective FFT plots.

### 4.1 Simulation Results for Sinusoidal Reference PWM

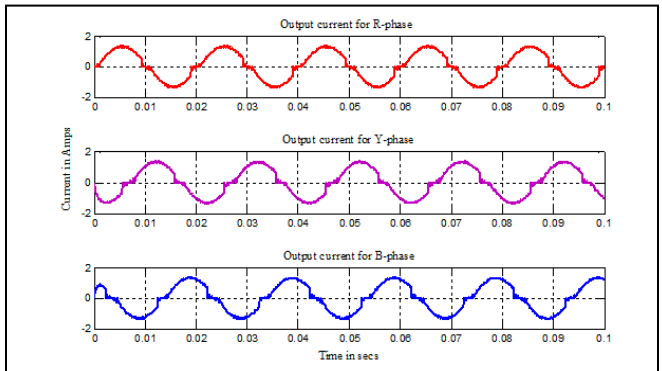


Fig. 4. Three-phase output current waveform for PDPWM tech-

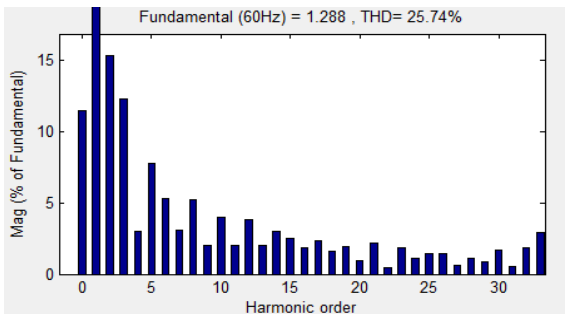


Fig. 5. FFT plot for output current of BPDPWM technique with sine reference.

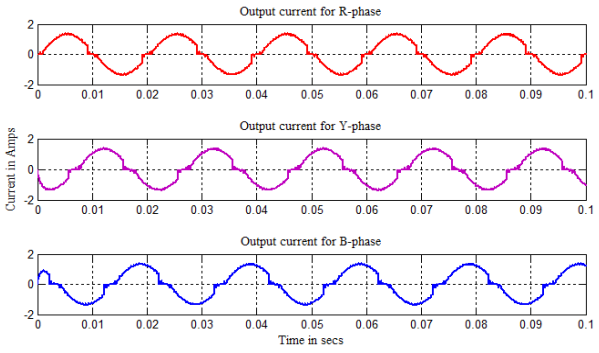


Fig. 6. Three-phase output current waveform for BPODPWM technique with sine reference.

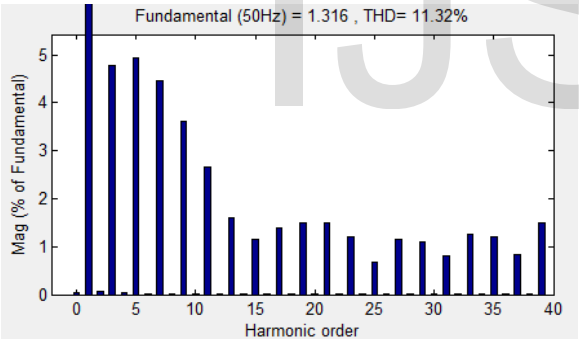


Fig. 7. FFT plot for output current of BPODPWM technique with sine reference.

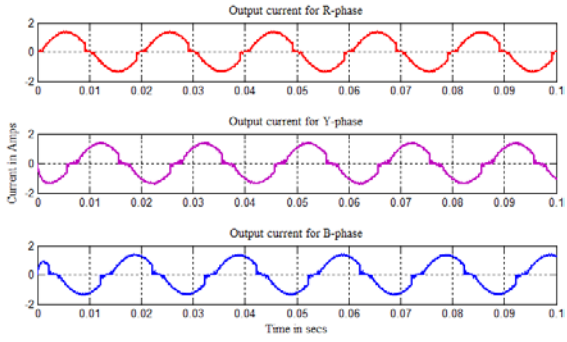


Fig. 8. Three-phase output current waveform for BAPODPWM technique with sine reference.

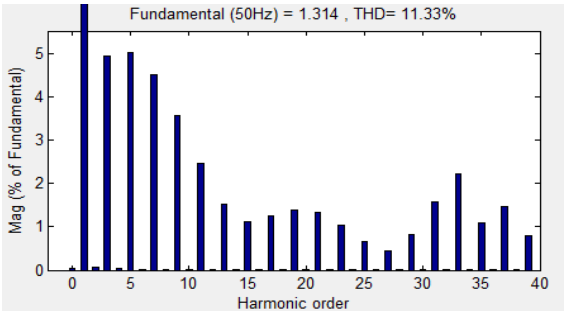


Fig. 9. FFT plot for output current of BAPODPWM technique with sine reference.

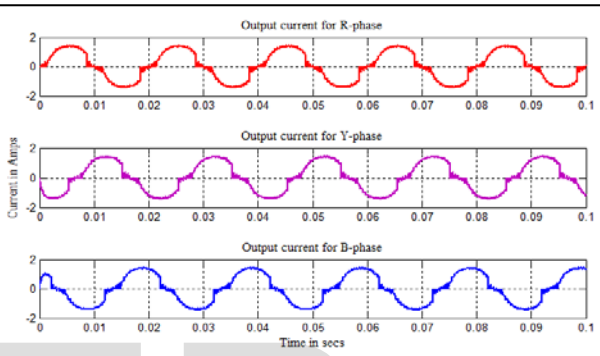


Fig. 10. Three-phase output current waveform for BCOPWM technique with sine reference.

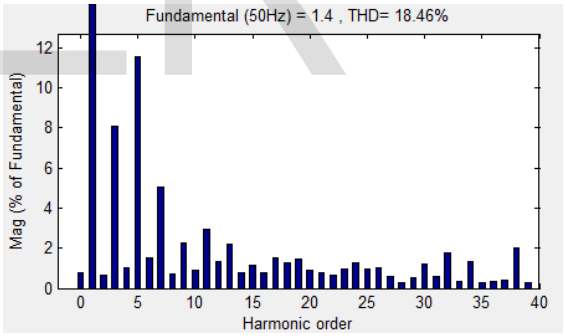


Fig. 11. FFT plot for output current of BCOPWM technique with sine reference.

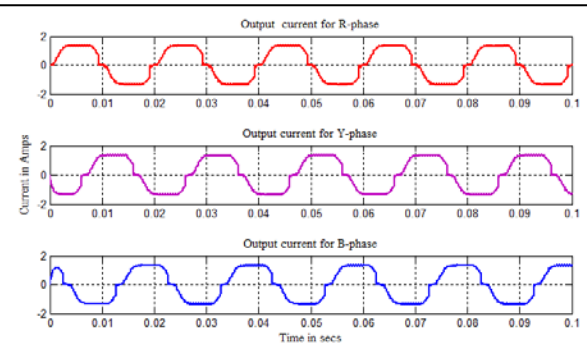


Fig. 12. Three-phase output current waveform for BVFPWM technique with sine reference.

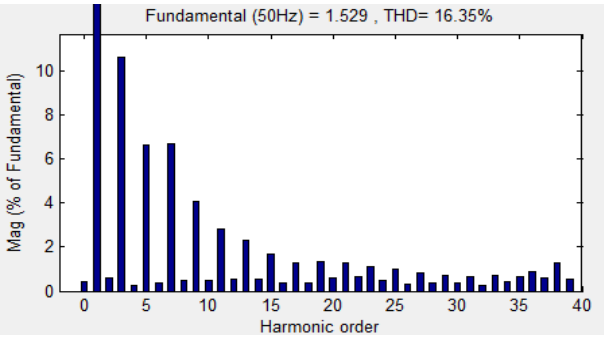


Fig. 13. FFT plot for output current of BVFPWM technique with sine reference.

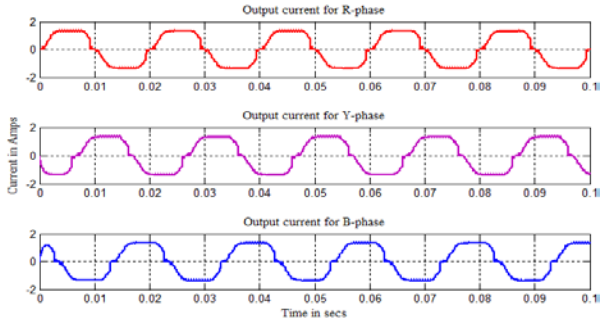


Fig. 14. Three-phase output current waveform for BPDPWM technique with trapezoidal reference.

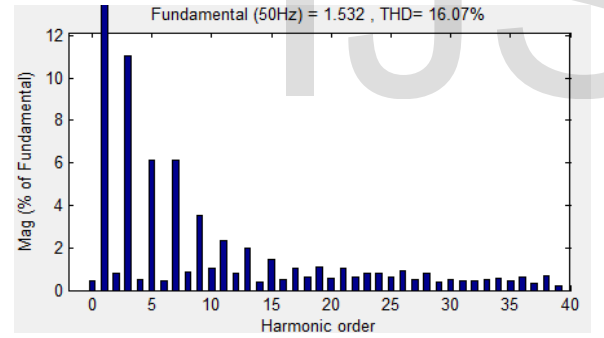


Fig. 15. FFT plot for output current of BPDPWM technique with trapezoidal reference.

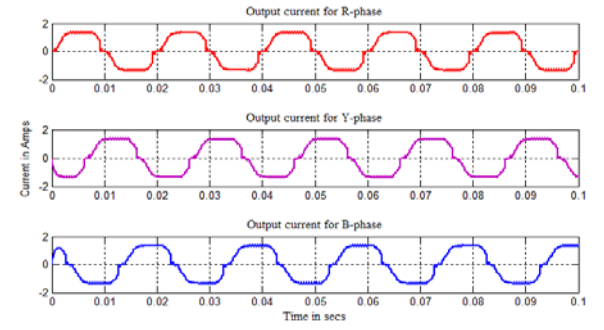


Fig. 16. Three-phase output current waveform for BPODPWM technique with trapezoidal reference.

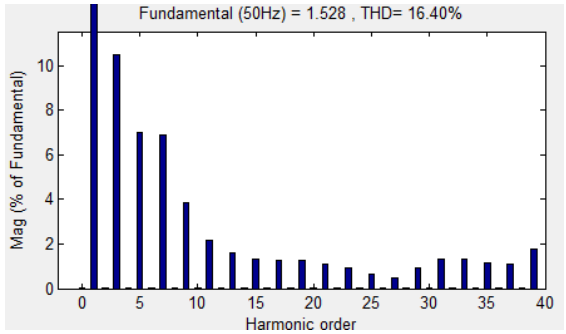


Fig. 17. FFT plot for output current of BPODPWM technique with trapezoidal reference.

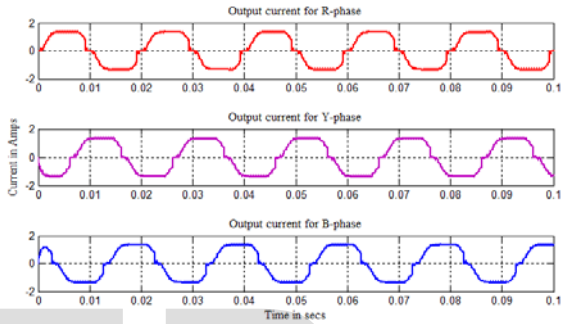


Fig. 18. Three-phase output current waveform for BAPODPWM technique with trapezoidal reference.

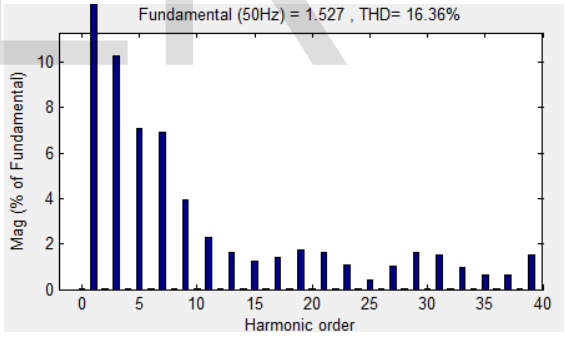


Fig. 19 FFT plot for output current of BAPODPWM technique with trapezoidal reference.

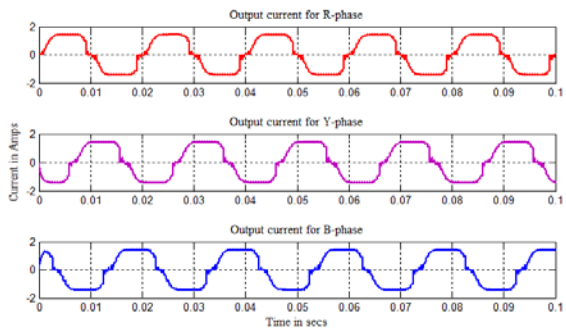


Fig. 20. Three-phase output current waveform for BCOPWM technique with trapezoidal reference.

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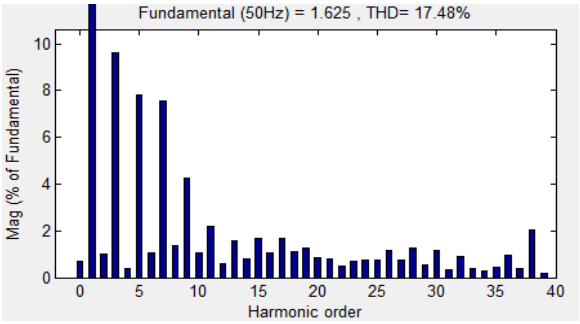


Fig. 21. FFT plot for output current of BCOPWM technique with trapezoidal reference.

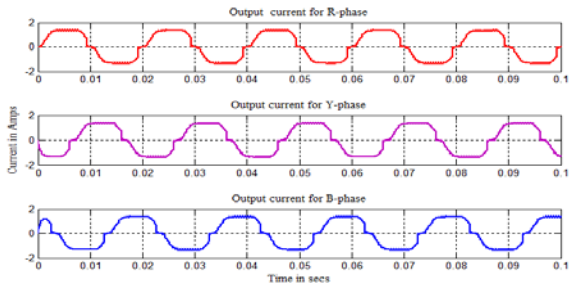


Fig. 22. Three-phase output current waveform for BVFPWM technique with trapezoidal reference.

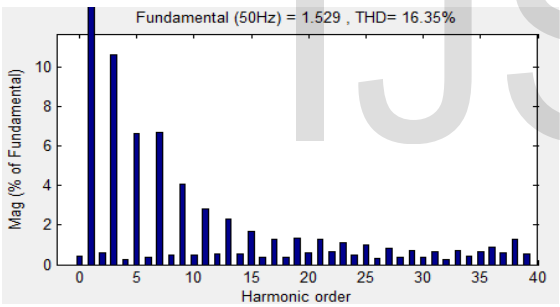


Fig. 23. FFT plot for output current of BVFPWM technique with trapezoidal reference.

TABLE 2
%THD FOR DIFFERENT MODULATION INDICES WITH SINE REFERENCE

| $m_a$ | PD | POD | APOD | CO | VF |
|---|---|---|---|---|---|
| 1 | 12 | 10.94 | 10.9 | 15.49 | 12.93 |
| 0.9 | 12.56 | 11.32 | 11.33 | 18.46 | 14.86 |
| 0.8 | 15.52 | 16.73 | 16.78 | 22.24 | 16.81 |
| 0.7 | 18.87 | 17.55 | 17.5 | 26.74 | 20.88 |

TABLE 3
$I_{RMS}$ FOR DIFFERENT MODULATION INDICES WITH SINE REFERENCE

| ma | PD | POD | APOD | CO | VF |
|---|---|---|---|---|---|
| 1 | 1.028 | 1.034 | 1.033 | 1.079 | 1.026 |
| 0.9 | 0.925 | 0.9307 | 0.9294 | 0.9899 | 0.9167 |
| 0.8 | 0.8121 | 0.8068 | 0.8069 | 0.8927 | 0.8083 |
| 0.7 | 0.6985 | 0.7037 | 0.7047 | 0.7764 | 0.6931 |

TABLE 4
$I_{PEAK}$ FOR DIFFERENT MODULATION INDICES WITH SINE REFERENCE

| ma | PD | POD | APOD | CO | VF |
|---|---|---|---|---|---|
| 1 | 1.454 | 1.462 | 1.461 | 1.526 | 1.45 |
| 0.9 | 1.308 | 1.316 | 1.314 | 1.4 | 1.296 |
| 0.8 | 1.148 | 1.141 | 1.141 | 1.26 | 1.143 |
| 0.7 | 0.9879 | 0.9951 | 0.9965 | 1.098 | 0.9802 |

TABLE 5
%THD FOR DIFFERENT MODULATION INDICES WITH TRAPEZOIDAL REFERENCE

| ma | PD | POD | APOD | CO | VF |
|---|---|---|---|---|---|
| 1 | 15.48 | 15.16 | 15.26 | 17.18 | 15.70 |
| 0.9 | 16.07 | 16.40 | 16.36 | 17.48 | 16.35 |
| 0.8 | 16.37 | 16.52 | 16.62 | 17.40 | 16.56 |
| 0.7 | 17.02 | 16.85 | 16.75 | 18.23 | 17.61 |

TABLE 6
$I_{RMS}$ FOR DIFFERENT MODULATION INDICES WITH TRAPEZOIDAL REFERENCE

| ma | PD | POD | APOD | CO | VF |
|---|---|---|---|---|---|
| 1 | 1.212 | 1.214 | 1.215 | 1.215 | 1.207 |
| 0.9 | 1.083 | 1.081 | 1.08 | 1.149 | 1.081 |
| 0.8 | 0.9695 | 0.9649 | 0.9655 | 1.095 | 0.9683 |
| 0.7 | 0.8395 | 0.8442 | 0.8438 | 1.024 | 0.8363 |

TABLE 7
$I_{PEAK}$ FOR DIFFERENT MODULATION INDICES WITH TRAPEZOIDAL REFERENCE

| ma | PD | POD | APOD | CO | VF |
|---|---|---|---|---|---|
| 1 | 1.212 | 1.214 | 1.215 | 1.215 | 1.207 |
| 0.9 | 1.083 | 1.081 | 1.08 | 1.149 | 1.081 |
| 0.8 | 0.9695 | 0.9649 | 0.9655 | 1.095 | 0.9683 |
| 0.7 | 0.8395 | 0.8442 | 0.8438 | 1.024 | 0.8363 |



## 6 CONCLUSION

The 7-level CMLI using eight switches is successfully introduced while the simulation done by MATLAB/ SIMULINK and observed a clear stepped 7-level waveform. Mainly found that the APODPWM strategy has lesser %THD while compared with all other PWM strategies for both references. The COPWM strategy is produce higher fundamental RMS output current. The new design is simple in its outlook and only few components were used. The novel 7-level multilevel inverter has lower THD compared to conventional symmetric and asymmetric topologies.

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